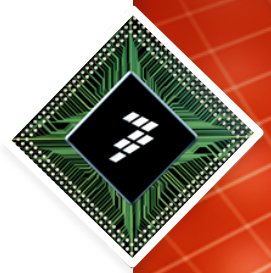
Freescale's Redistributed Chip Packaging

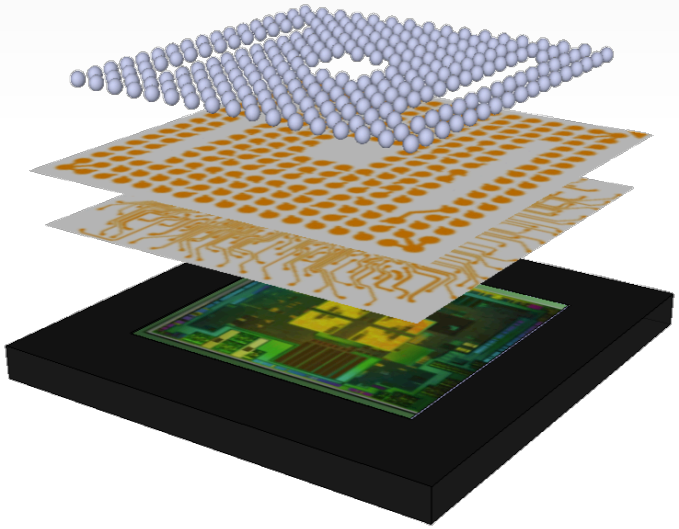
(RCP)

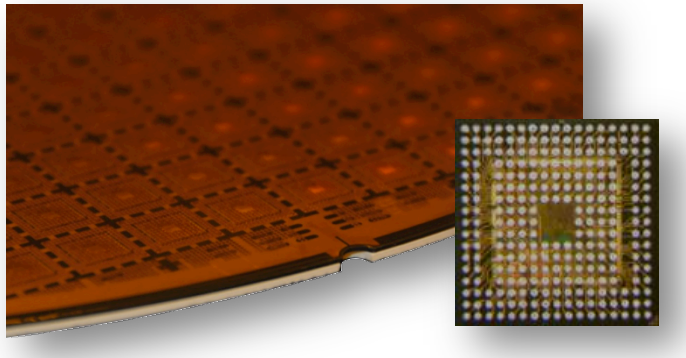


Jan 2013

Freescale Redistributed Chip Packaging

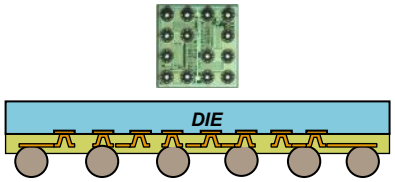
- Freescale proprietary technology
- Scalable, fan-out chip scale package
- A technology solution for:
  - Small form factor packages
  - High performance
  - Multi-die, heterogeneous integration
- 2D, 3D System in Package (SiP) solution
- Key applications
  - Medical
  - Defense
  - Migrate to consumer, industrial and auto



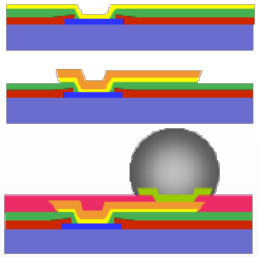


WLCSP vs. RCP

WLSCP

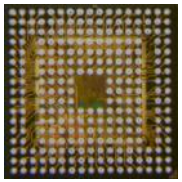


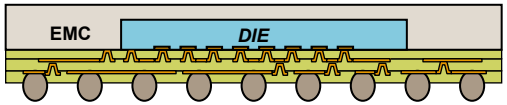
- Blind assembly directly on a wafer
- Pkg size = die size

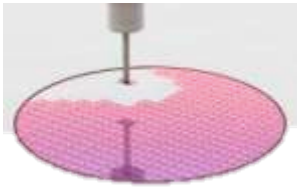


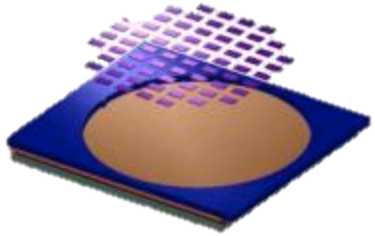
- Build up process based on bumping technology
- Single redistribution layer (RDL)
- Exposed back side and edge of die

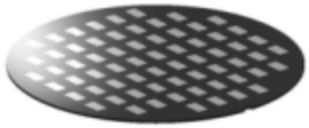
RCP



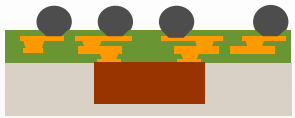








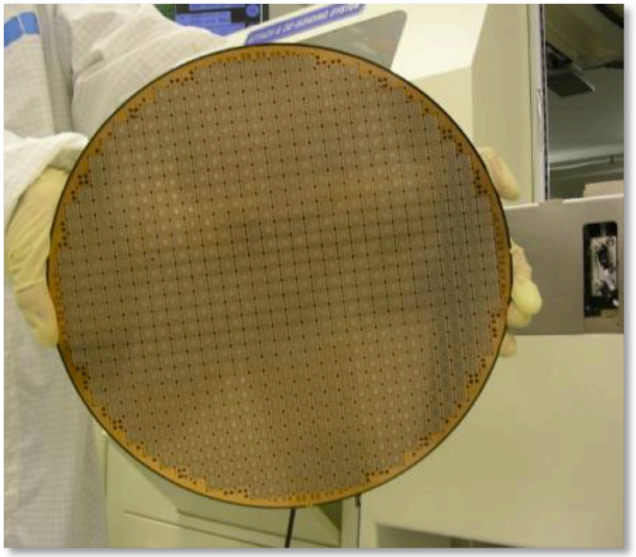
- Wafer reconstitution with KGD / Probed die
- Space creation to accommodate more I/Os, sophisticated routing and heterogeneous integration



- Build up process with fan-out routing
- Multiple RDLs
- Physical protection for die

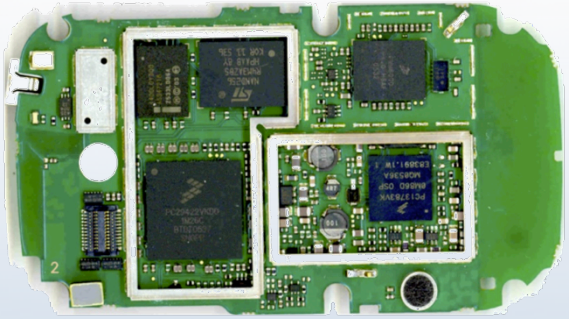
About Freescale Redistributed Chip Packaging

- Package size reduction
- Cost competitive, high productivity, large area batch process
  - Eliminates package substrate
  - Eliminates gold wire bonds/C4 bumps
- High-performance package
  - Reduced electrical parasitics
  - Higher frequency response
- Ultra low-k compatible (<90 nm MLM)
  - Compliant with advance Si technology
- Pb free, halogen free, ROHS compliant
- Single chip, multiple chip and embedded component capability
- 3D IC enabling with system integration roadmap
- Certified to JEDEC/FSL commercial, industrial, automotive level reliability at the high volume manufacturing site



9 x 9 mm packages
258 I/O, 0.5 mm pitch
716 packages/panel
Two layer build-up

Where RCP Provides Significant Value



45 x 90 mm

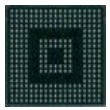
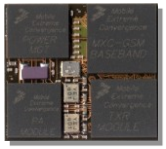
- 440 peripheral components
- 10-layer PCB

30 x 30 mm

3G-UMTS Radio

- 86 embedded peripheral components
- 36 SMT peripheral components
- Total of 122 peripheral components
- Does not include PA or power FETS
- 3- to 4-layer PCB required for HIF

75% reduction in area • 70% peripheral components eliminated

Miniaturization	Integration	Elimination
 13 x13 mm MBGA  9 x 9 mm RCP		
• 30-80% area reduction (system dependant) • Eliminates wire bonds and substrate • Maintain same ball pitch or smaller • 30% thinner than standard BGA	• Multiple die, any device technology • Die plus peripherals in package • 3D with other packaging technologies • SMT actives and passives on top	• Replace majority of motherboard • Significant peripheral components elimination • Eliminates wire bonds and substrate from package

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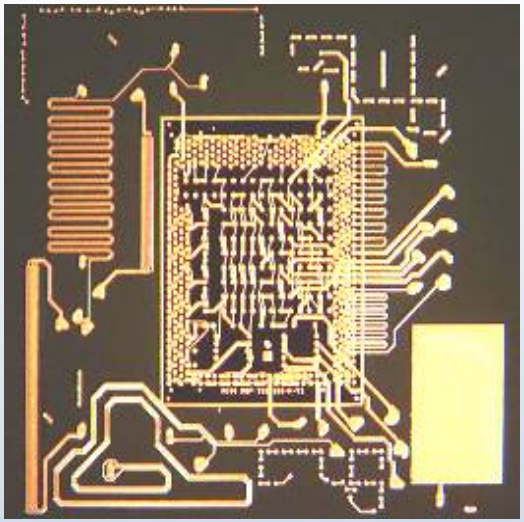
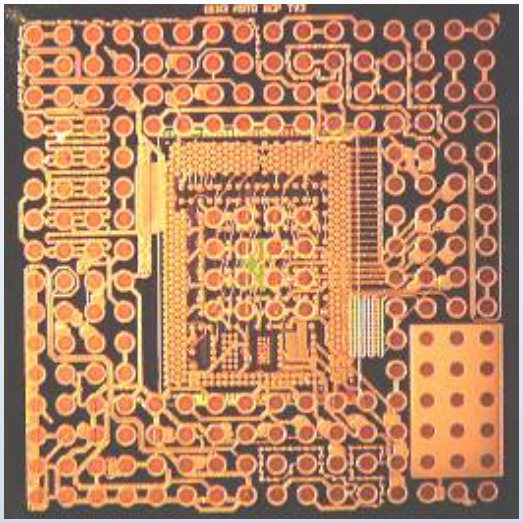
RCP Build-Up Process

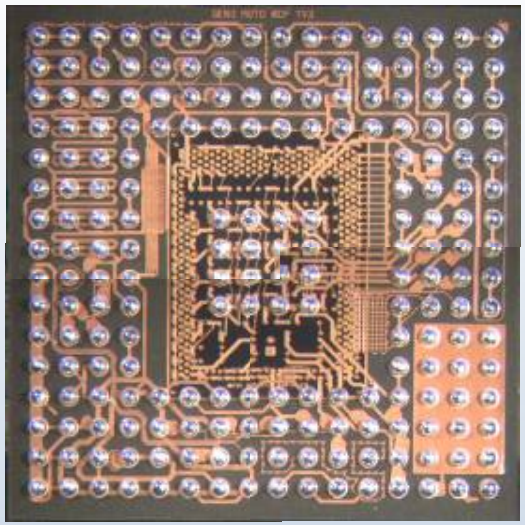
Metal 1 Layer



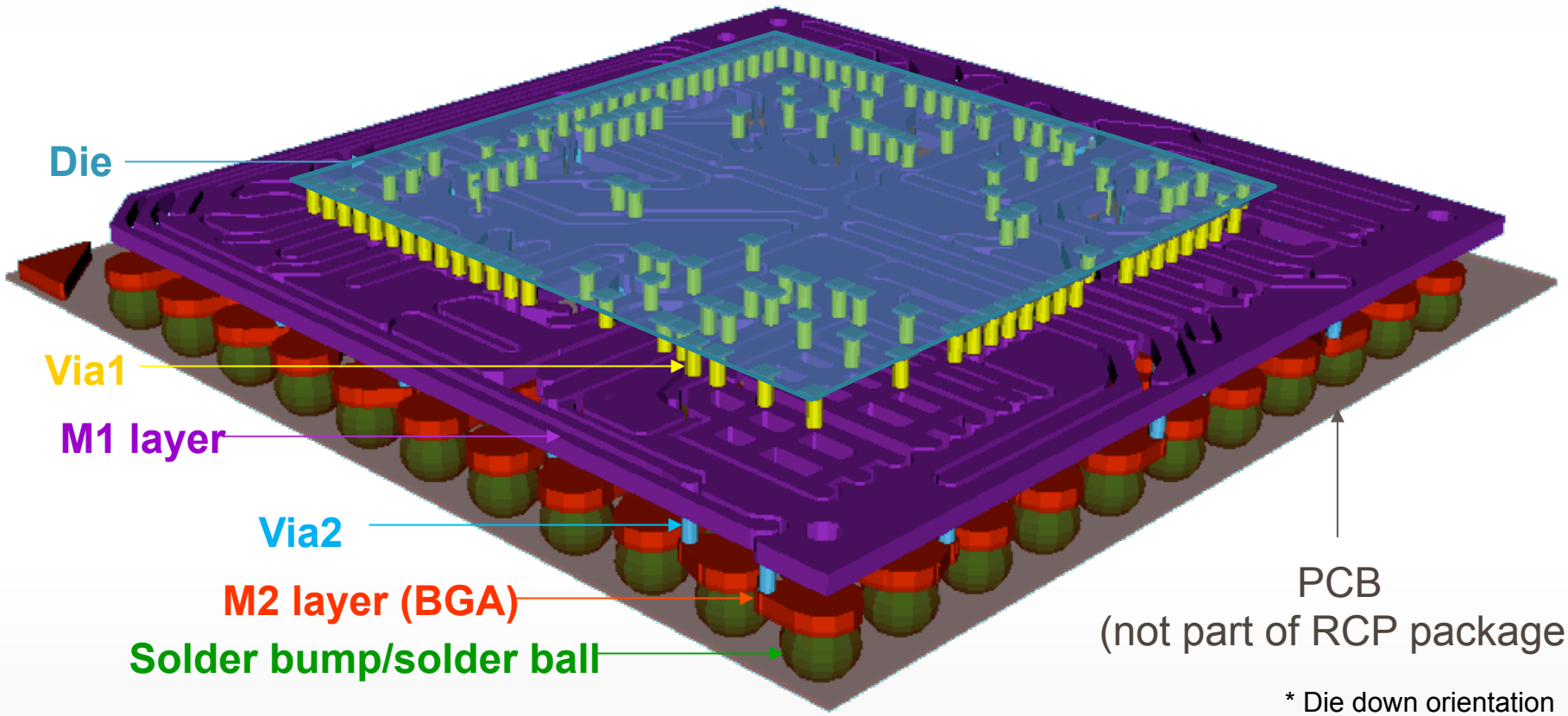
Metal 2 Layer



BGA

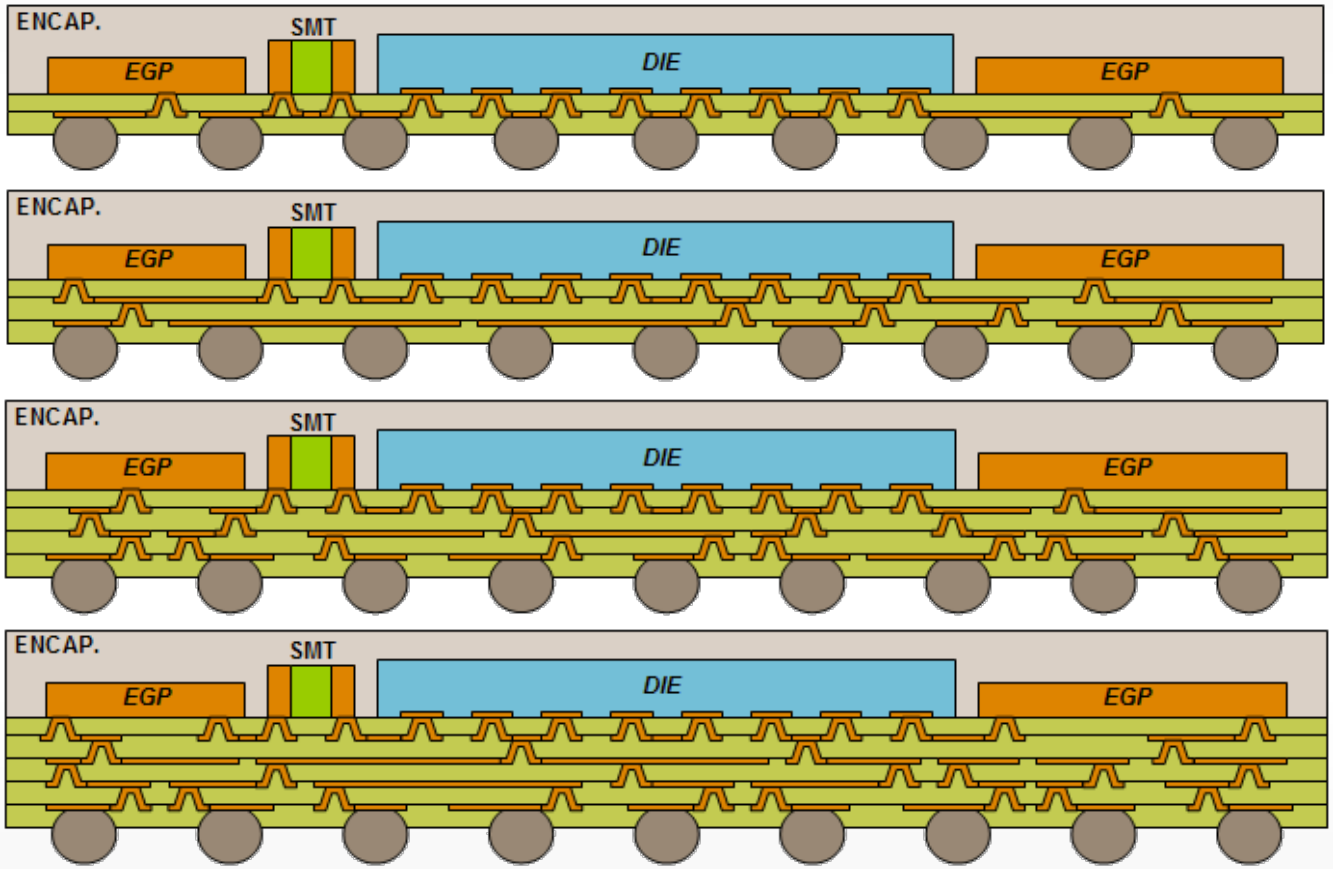


2ML RCP Package Construction



* Die down orientation

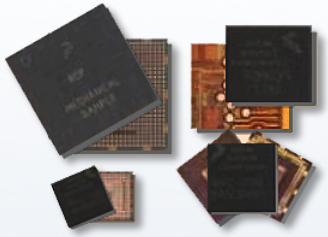
Single-Sided RCP



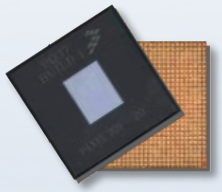
Build-up dielectrics and metallization are constructed using photolithography and plating process

RCP Packages Built

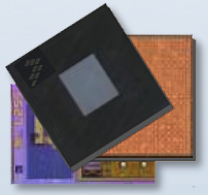
Single Sided Build Up Single Die



2G, 3G, Baseband, Power Management

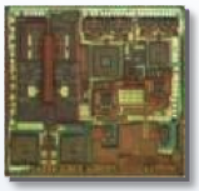


Power Control

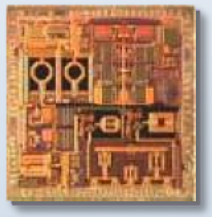


DSP

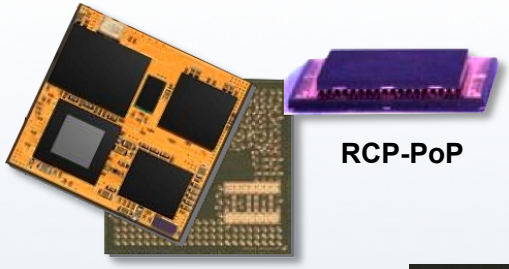
Single Sided Build Up Multi Die, SMT



PA, TxRx, RF Modules

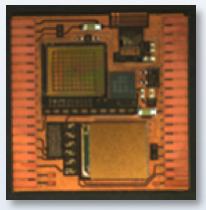


Double Sided Build Up RCP Stacking System Integration



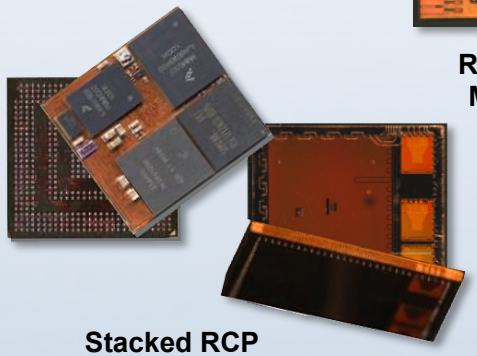
RCP-PoP

2.5G Radio-in-Package



3G Radio-in-Package

RCP-3D MEMS



Stacked RCP

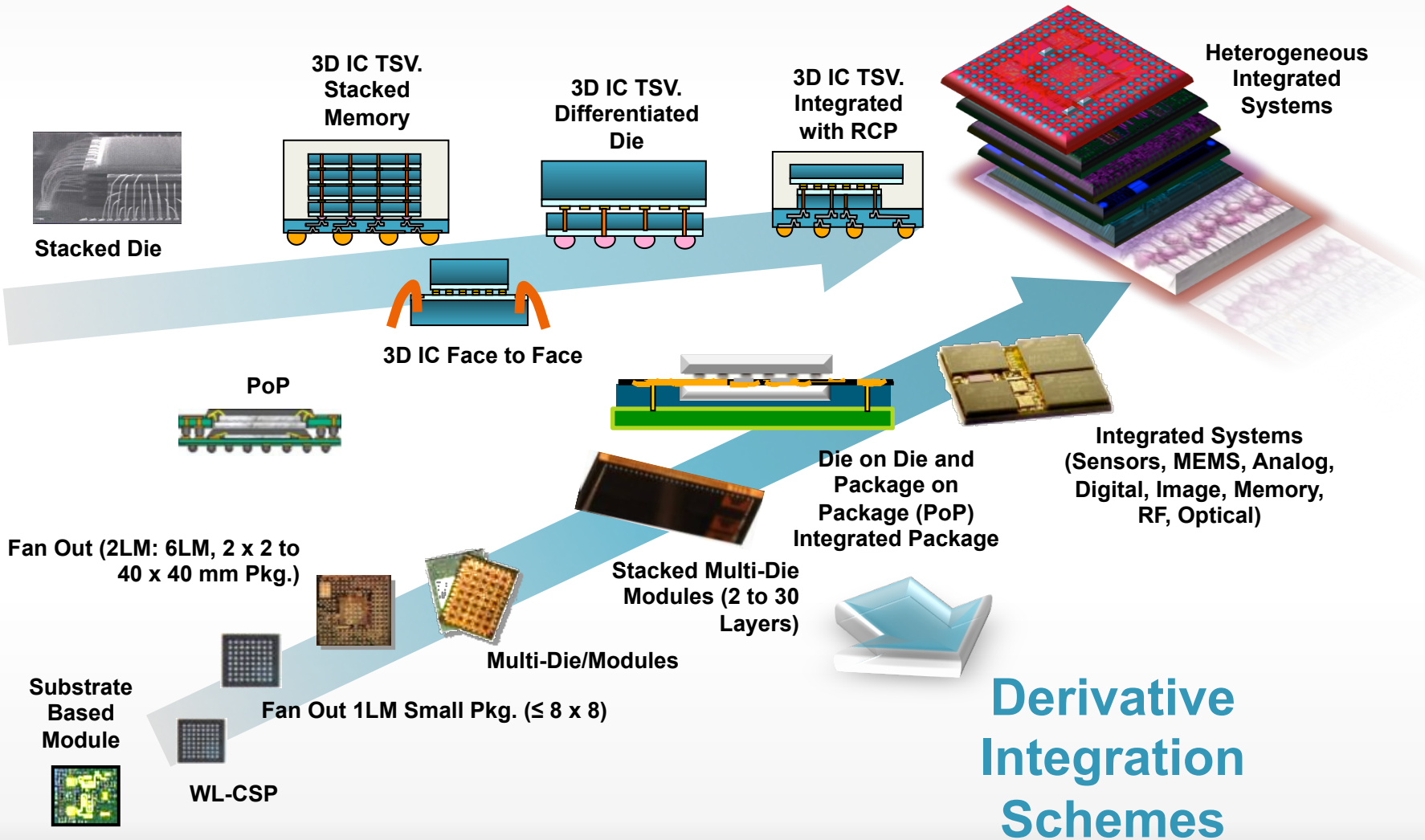
2ML

Increasing Metal Layers

4ML

2D → Increasing Integration → 3D → Stacking

Convergence of 3D with RCP Integrated Systems



Derivative Integration Schemes

System in Package (SiP) Industry Thrust

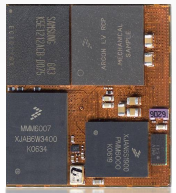
SiP addresses a potentially large need in the market and is being recognized as the next industry thrust.

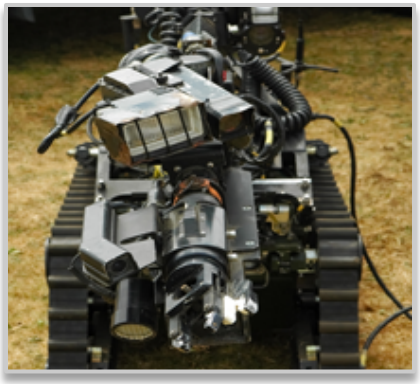
- Heterogeneous integration
- System miniaturization
- System performance
- High speed in package computing
- System flexibility (chip sourcing, integration)
- Block testability
- Path to integrating with 3D IC

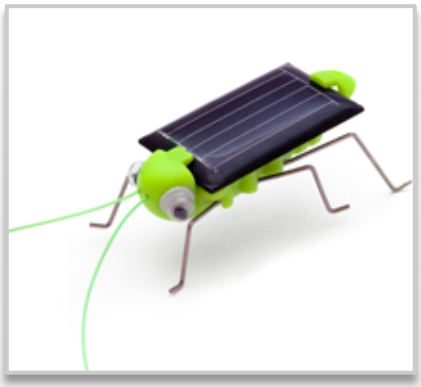
Game Changing Opportunity with RCP SiP

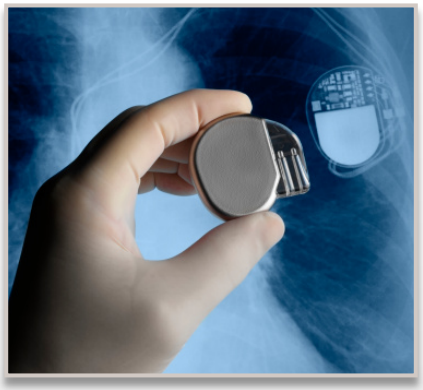
- Targeting 40-80% shrink over today's solutions
- Integration of heterogeneous IC
  - Ultra-thin, high-density stacked capacitors
  - Low- and high-voltage devices
  - IPDs
  - RF devices
  - ASIC and MCUs
  - Memory
  - MEMS devices
  - Integration of optical devices and interconnects
  - Replace PCB with all components built in RCP
- Single-die, multi-die 2D, 3D, ultra-thin and stacked packages
- BGA, micro-BGA, flex connectors, wire bond
- Targeting active devices
- Developing small, passive, monitoring devices
- Contactless or proximity charging devices

A Few of the Targeted Applications of RCP

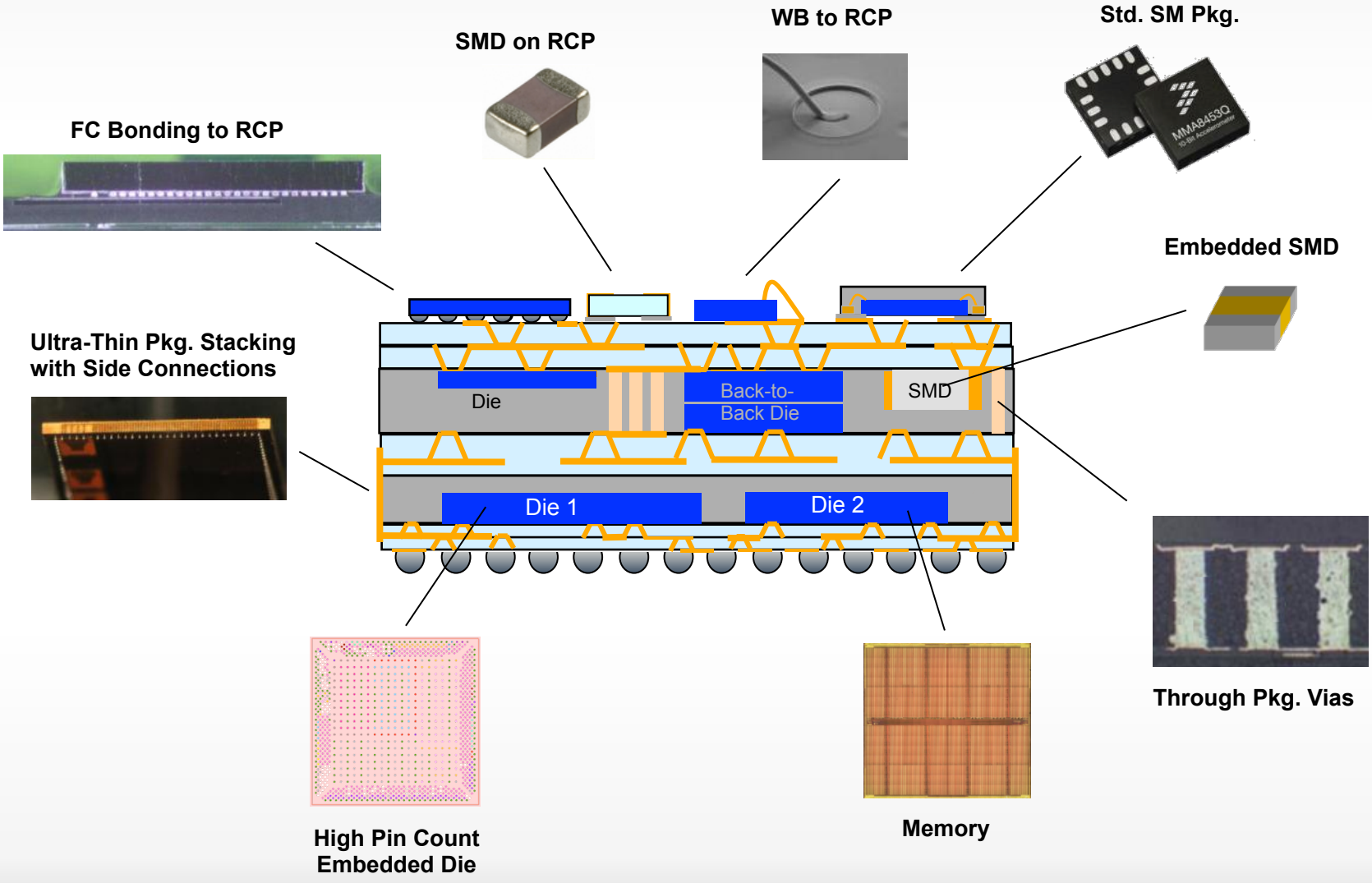








RCP Building Blocks

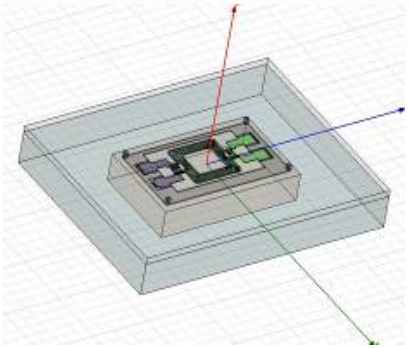


RCP 2D SiP

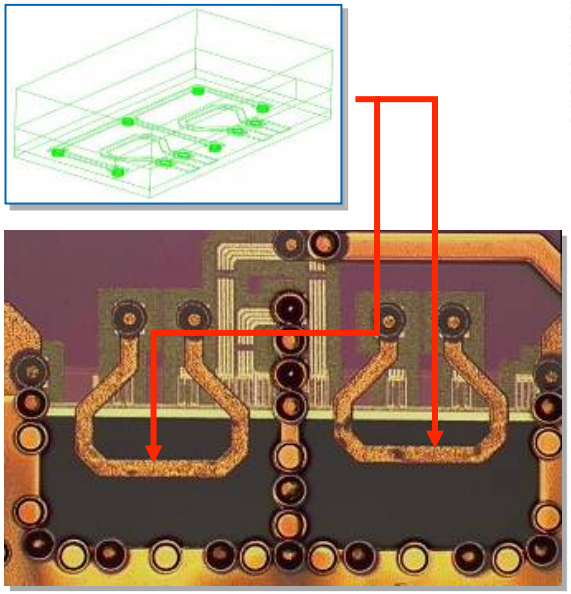
RCP SiP Possibilities

- Multi die
- Embedded SMTs
- Active RF features
- Shielding
- Shortened design cycle
- Improved performance

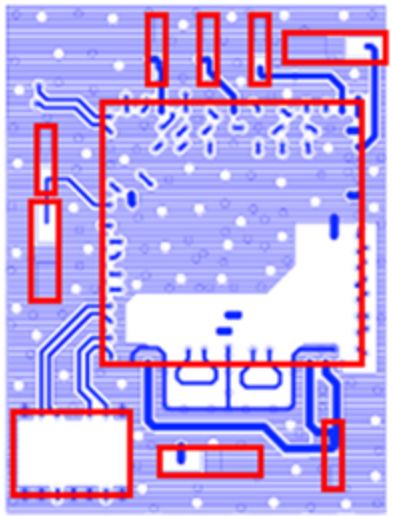
Balun in RCP



VCO Coils RCP



Transceiver RCP



- ~30% size reduction over HDI
- ~40% cost reduction over HDI
- Improved performance over HDI through better signal isolation

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RCP Development: Multi-Die/SiP

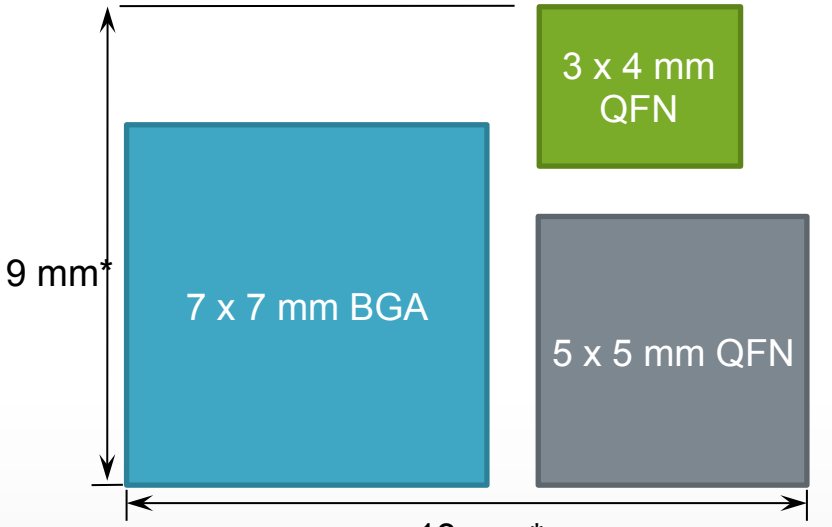
Existing Separate Package Solutions

Product	Packaging Area mm²	Packaging Type
Audio Codec	25.00	QFN-EP
USB	12.00	QFN-EP
PMIC	49.00	MapBGA
Total	**86.00**	

Compare package area only

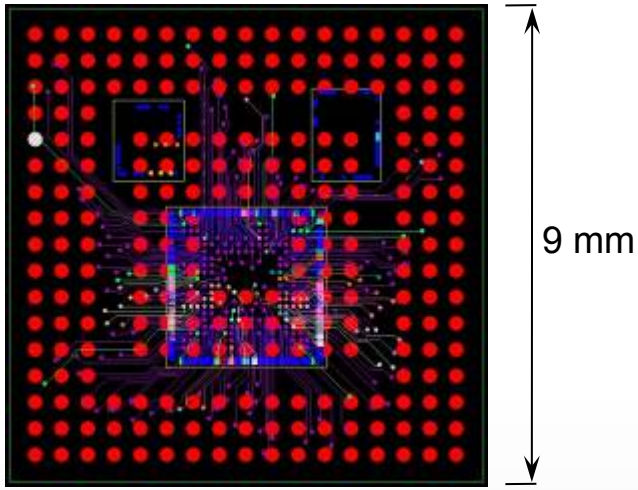
RCP Solution

- 9 x 9 mm, 0.5P
- 81 mm²
- Several SMTs to be included in this space



Compare total packaging area

117 mm² > 81 mm²
~30% reduction in area



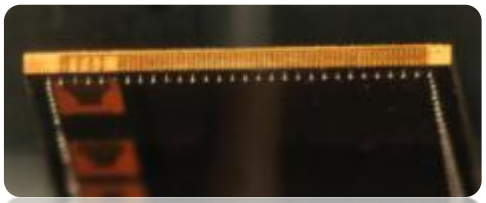
*Assumes 1 mm spacing between packaging on app board

Space savings to exceed 30%

3D RCP: Enabling Structures

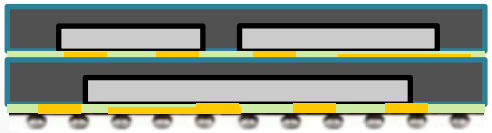
Layer Stacking and Side Metal Interconnect

- 3D structure created by laminating two or more RCP layers
- Connections formed by wrap around leads
- Ultra thin profile



3D RCP SiP

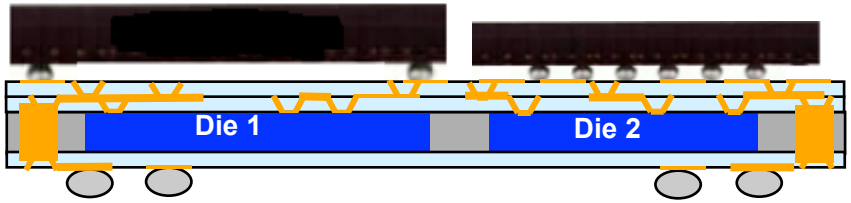
Ultra Thin RCP

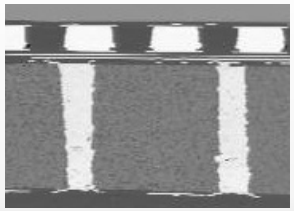


Two Laminated Layers and Side Metal Interconnect

Two-Side Build Up with Through-Package Via

- Two-sided build up enables mounting on both sides of package
- Vias in package allows for PoP
  - Higher interconnect density
  - Improved electrical parasitics (shorter wiring lengths)
  - Simplified designs (die size disparity)





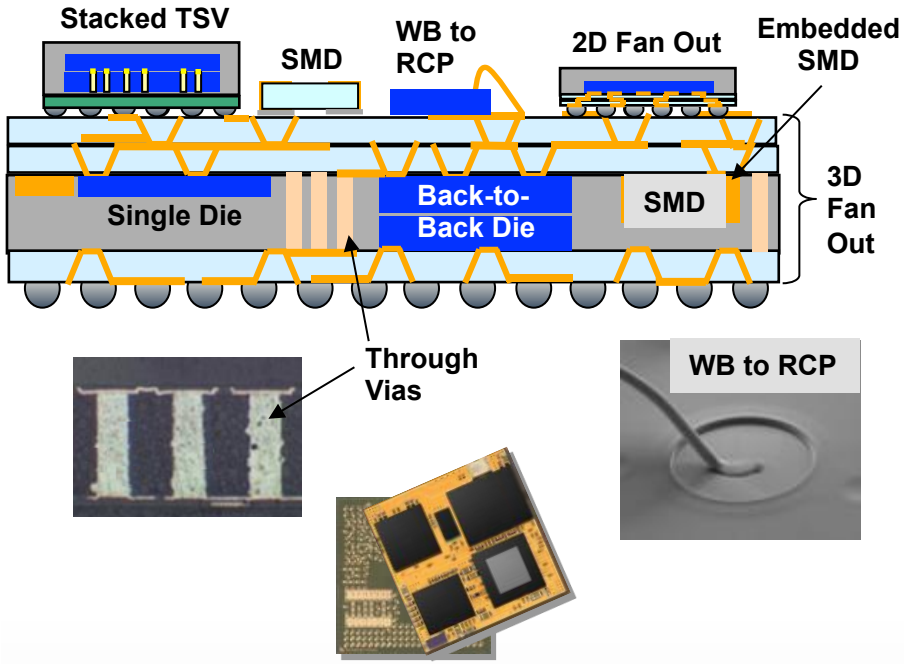
3D RCP: Enabling Structures (continued)

Face-to-Face Integration

- Similar to structures in traditional SiP packaging
  - Allows for a very low height stack

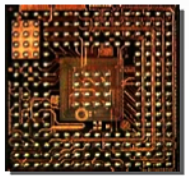
- Enables extremely high bandwidth between two chips
  - Key application: MPU and memory integration

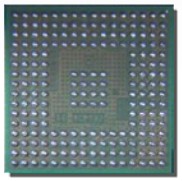
SiP Integration

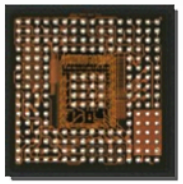


- Similar to structures in traditional SiP packaging
  - Enables test and supply chain simplification
  - Improved volumetric efficiency
  - True heterogeneous integration

RCP Test Vehicles and Assembled Products


TV1


TV2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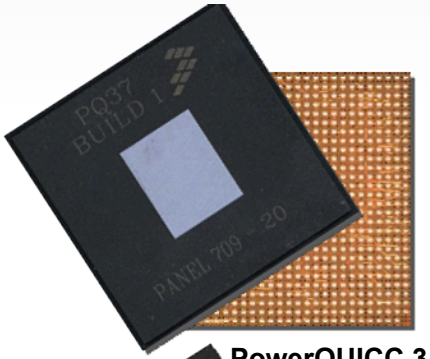
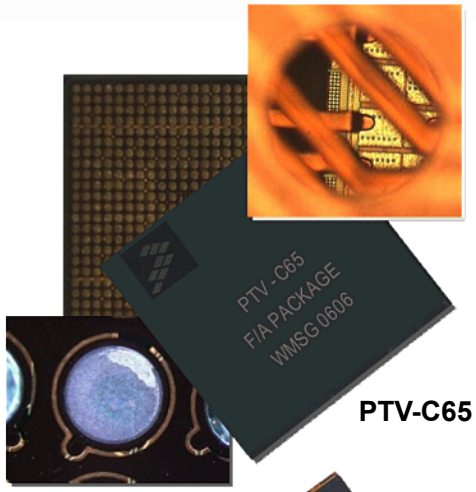
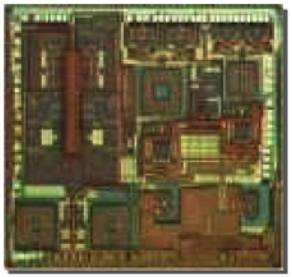
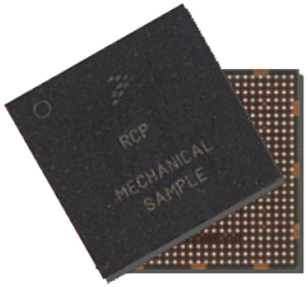


PowerQUICC 3

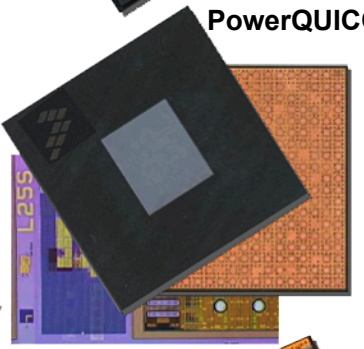


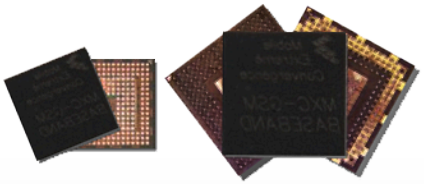
PTV-C65

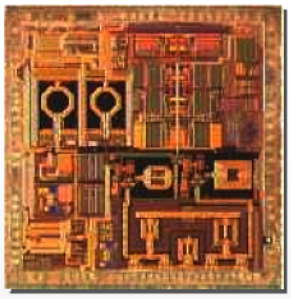

PA Test Vehicle



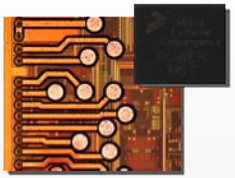
3G Baseband

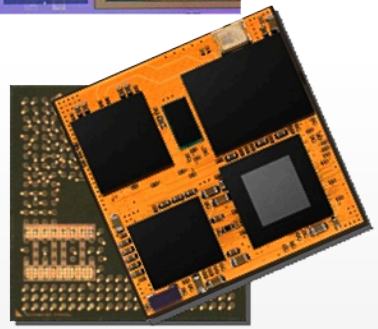

Network Processor

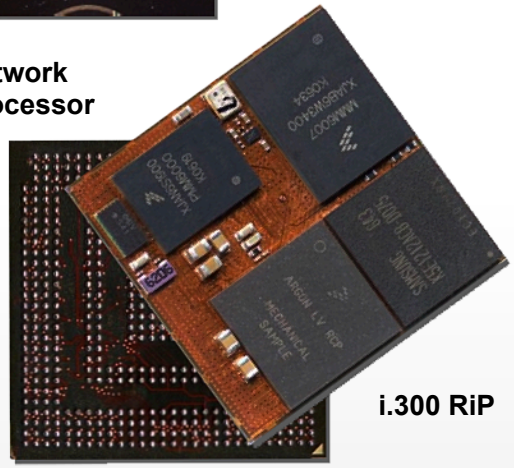

2G Baseband


RF Test Vehicle


XTR


Power Management


i.275 RiP



i.300 RiP

Additional RCP Discussion and Support

Additional technical details and following specific supports are available. Send the request to freescale.com/webapp/sps/site/overview.jsp?nodeId=062874425677 52

- Technology details and design rules
- Package design, electrical, mechanical and thermal modeling
- Discussions on application-specific solutions and options
- Customer-specific RCP SiP solutions
- Design and fabrication of prototypes from Freescale Tempe RCP line
- Path to production

Or with following contacts:

Mail to:
Director
Foundry Services Organization
Technology & Manufacturing
Freescale Semiconductor
6501 William Cannon Drive West
MD OE329
Austin, Texas 78735-8598

Or fax to:
Attention—Director of Foundry Service Organization
(512) 895-7134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